TIEμ

2nd Edition

Technologies of Interconnections in Electronics
Advanced Packaging Challenge

Transilvania University of Brasov

2nd - 5th April 2024

Why IC packaging?

- ❑ Every chip needs a package
- ❑ Packaging interconnect complexity increasing over time
- ❑ Advanced packaging and chiplet technology already is a differentiator

TIEμ

A competition designed focused on advanced packaging, layout and associated electrical simulations

Objectives:

- ❑ Showcase the world of IC packaging to aspiring students
- ❑ Create a collaborative ecosystem between industry, academia and EDA vendors
- ❑ Enable tackling more complex problems, such as 2.5D packaging and chiplets

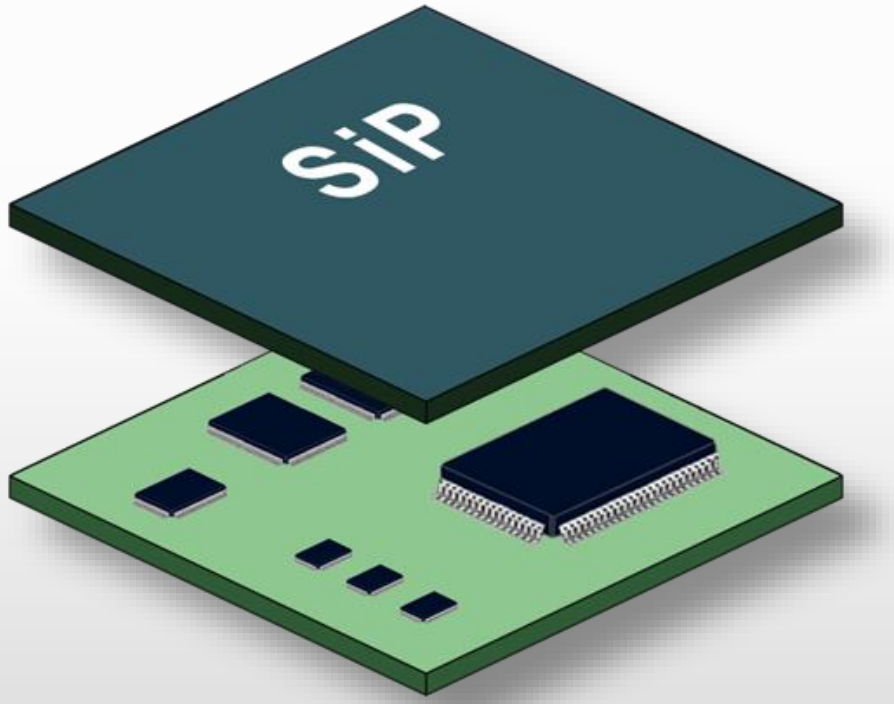


Figure By Verdel - Own work, CC BY-SA 4.0, https://commons.wikimedia.org/w/index.php?curid=97700648

APTE iMAPS ROMANIA UPSEE UP-SKILL ENGINEERING EDUCATION MICROCHIP NXP

TIEμ 2nd Edition

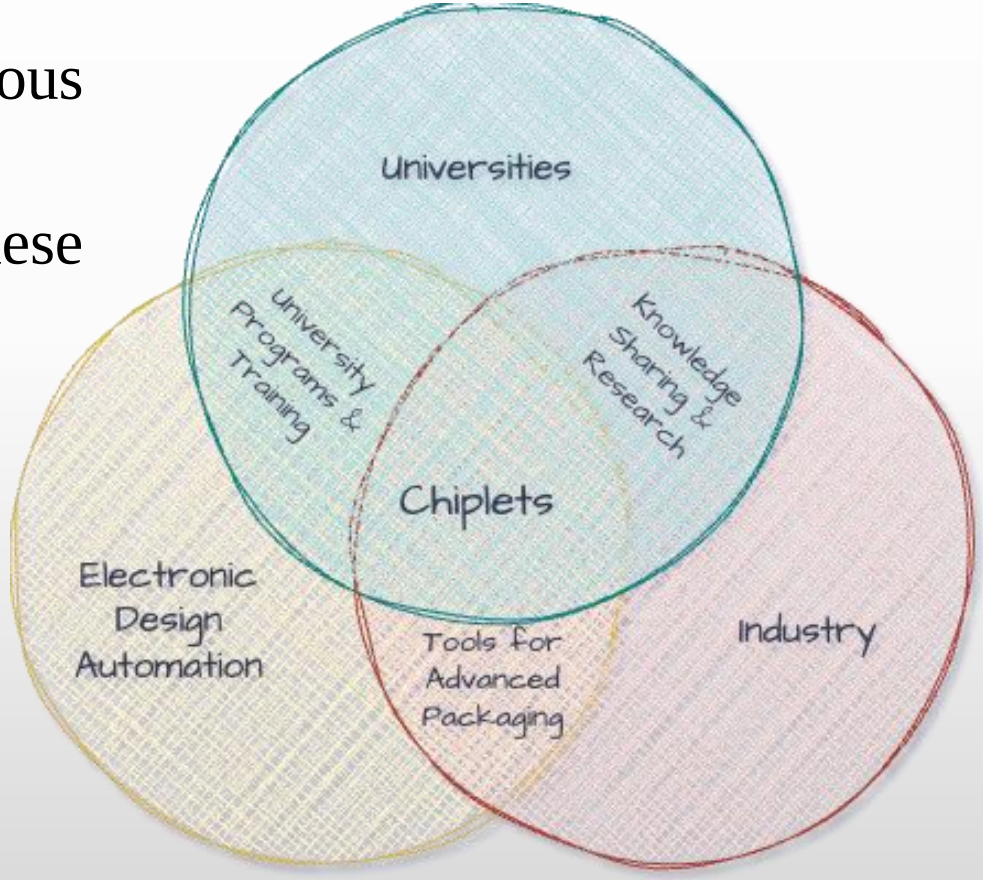
Technologies of Interconnections in Electronics

General Objectives

Transilvania University of Brasov

2nd - 5th April 2024

- Industry shifts towards heterogeneous integrations, SiP, chiplets
- Important to train future engineers in these techniques
  - Interposers
  - 2.5D, and 3D integration



General Objectives

TIE-μ focuses (long term) on the new interconnection challenges

- High-speed interfaces
- Interposers

- Prepare students when transitioning from SoC to SiPs

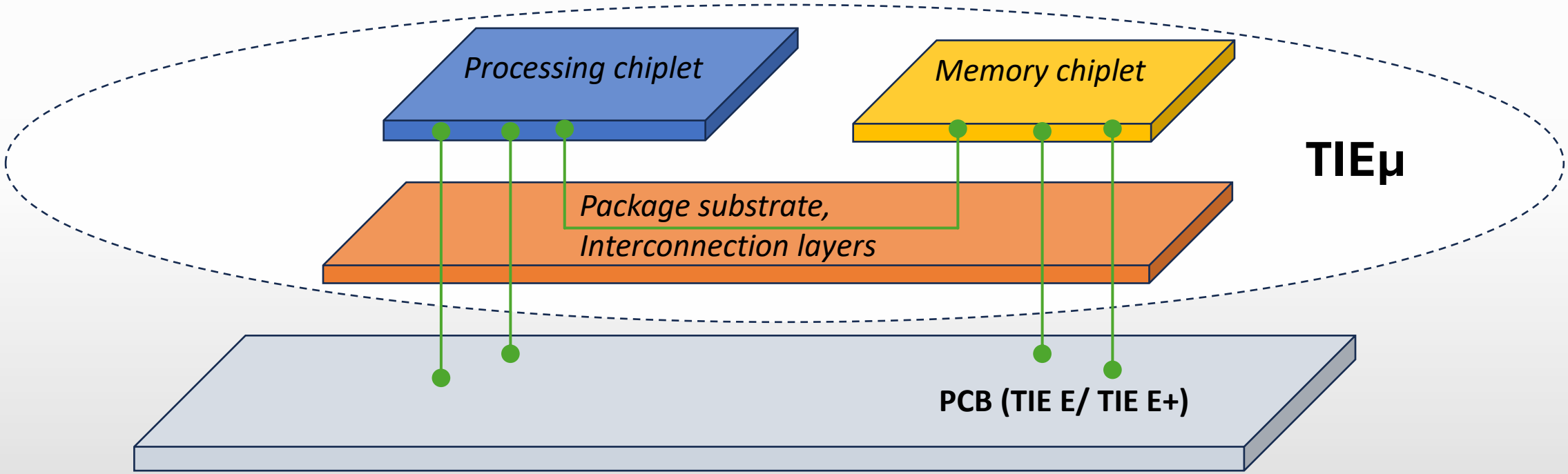
- SiPs – integrates on the same package
  - Specialized chiplets with customer IP
  - Memory
  - Processing units
  - Passive components

TIEμ 2nd Edition

Technologies of Interconnections in Electronics
Architectures

Transilvania University of Brasov

2nd - 5th April 2024



TIEμ 2nd Edition

Technologies of Interconnections in Electronics

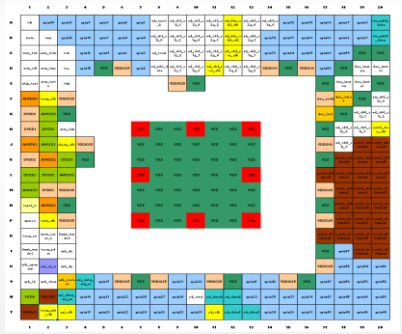
Package Design Workflow

Transilvania University of Brasov

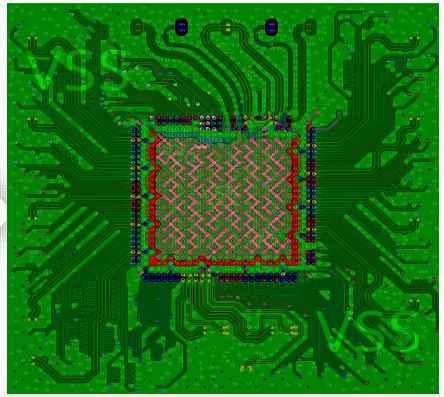
2nd - 5th April 2024

Customer Requirements

Floorplan



Package Netlist



Package Layout

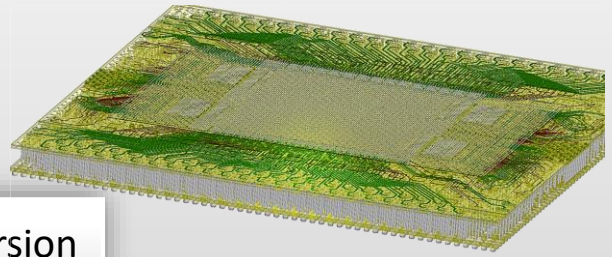
Signal & Power Integrity

cadence

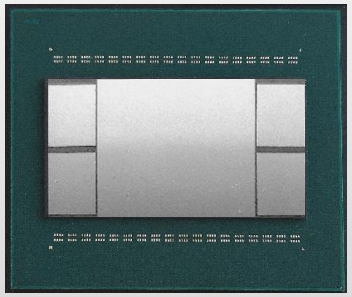
ANSYS

SYNOPSYS

Advanced Design System



Final Version



Final Product

APTE iMAPS ROMANIA

UPSEE UP-SKILL ENGINEERING EDUCATION

MICROCHIP

NXP

TIEμ 2nd Edition

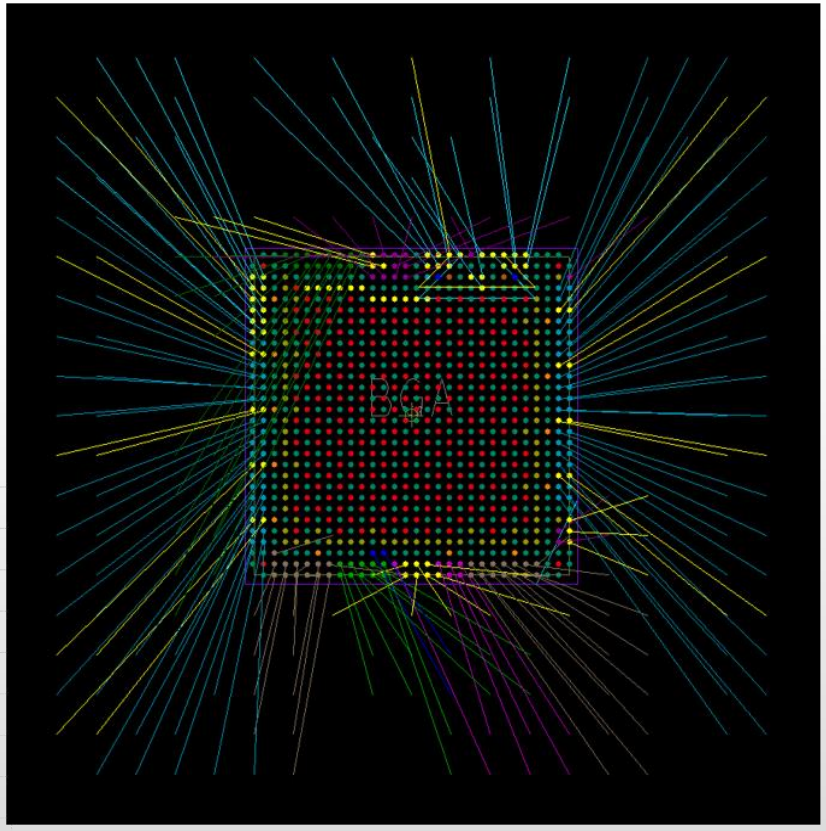
Technologies of Interconnections in Electronics

Task A. Substrate layout (2024)

Transilvania University of Brasov

2nd - 5th April 2024

- Check and update netlist based on the input files
- Complete layout electrical connections (no unconnected nets)
- All PDN connected to ensure a low resistance path from BGA to Bumps
- Continuous return path for high-speed signals: PCIe VSS return path and DDR3 signals VSS & VDD return path
- All signals routed as short as possible, if not otherwise stated, to minimize signal attenuation
- High speed PCIe signals need to be shielded from other signals. Signal routing length can be added to decuple adjacent differential pairs if SI IL specification are met
- All signal traces should have as much stitching vias as possible to create shielding
- DFM aspects: A1 mark, fiducials, degassing holes



APTE iMAPS ROMANIA UPSEE UP-SKILL ENGINEERING EDUCATION MICROCHIP NXP

TIEμ 2nd Edition

Technologies of Interconnections in Electronics
Task B. Power Integrity (2024)

Transilvania University of Brasov

2nd - 5th April 2024

I. Evaluate Structure IR Drop and Electric capabilities

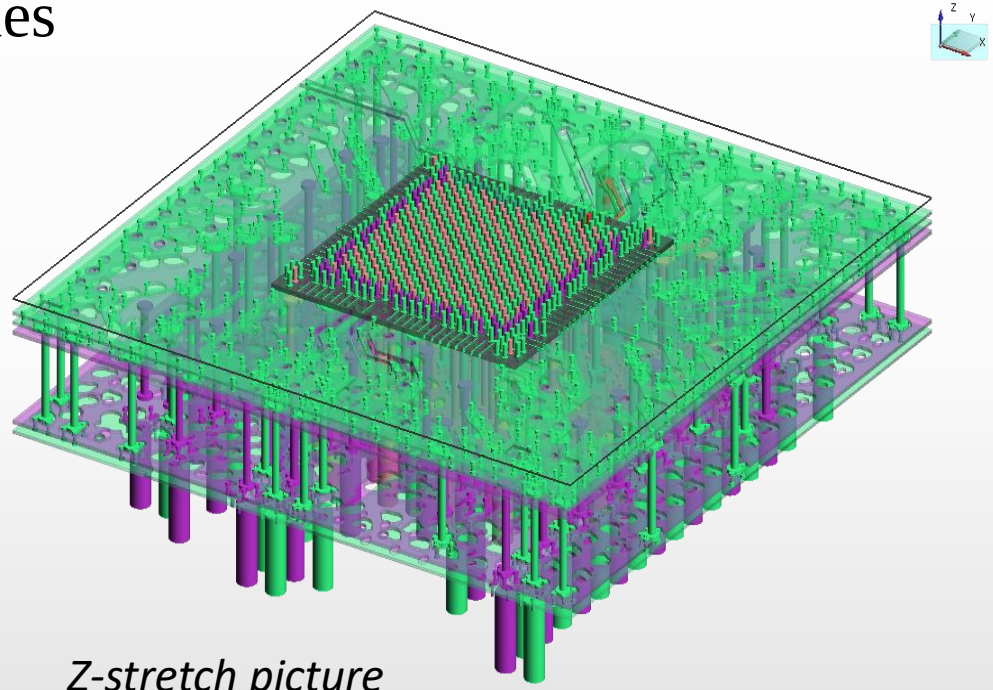
- ❑ Create a valid setup using package properties and simulation conditions
- ❑ Simulate and Check IR Drop values and Interconnects Electric capabilities
- ❑ Investigate using results weak spots in design and optimize layout to pass
  - ❑ IR drop spec
  - ❑ E-Constraints spec

II. Check nets RL per pin on Die side component

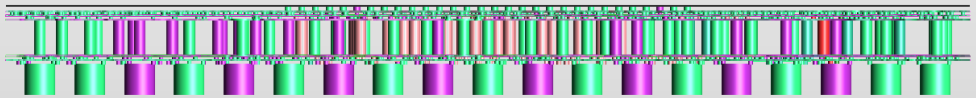
- ❑ Create a valid setup using package properties and simulation conditions
- ❑ Simulate initial results and verify R-DC and L-self against specifications
- ❑ Enhance layout and redo simulation until specification passed per each net

III. Setup and Verify Impedance curve trend

- ❑ Create a valid setup using package properties and simulation conditions
- ❑ Simulate initial result and verify package only impedance at Die
- ❑ Overlap impedance mask and check for violation on each rail
- ❑ Optimize layout and redo simulation so inductance trend not violate spec



Z-stretch picture



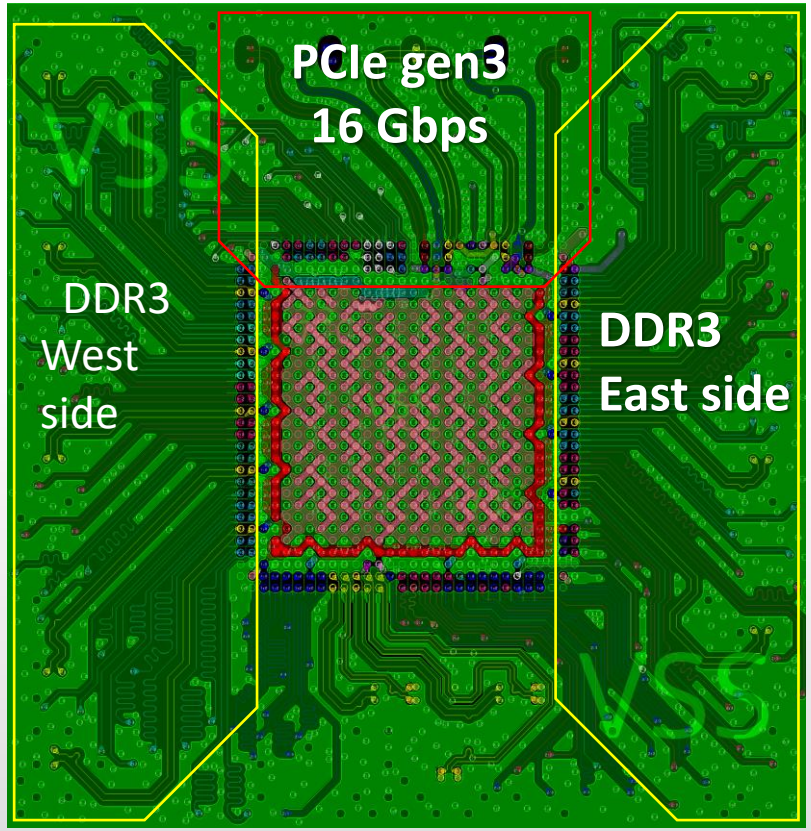
APTE iMAPS ROMANIA UPSEE UP-SKILL ENGINEERING EDUCATION MICROCHIP NXP

TIEμ 2nd Edition

Technologies of Interconnections in Electronics
Task C. Signal Integrity (2024)

Transilvania University of Brasov

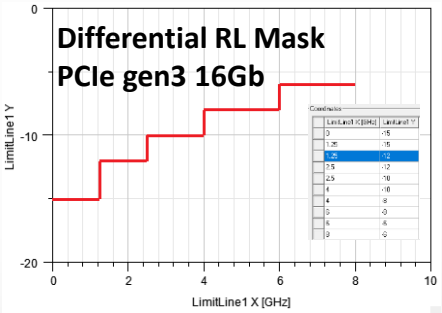
2nd - 5th April 2024



(Illustration of the actual TIEμ 2024 Subject)

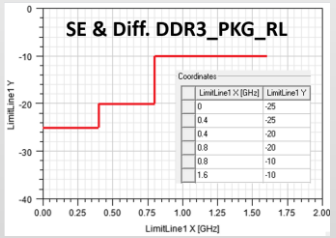
PCIe gen3: 100ohm interface @ 16Gbps

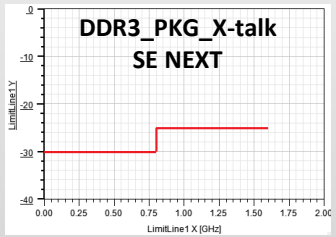
- ❑ S-parameter model extraction of the PKG routing with sufficient bandwidth
- ❑ Report SI results of the initial layout vs. PKG requirements (masks)
  - ❑ Differential Insertion Loss (IL) & Return Loss (RL)
  - ❑ Differential & Single Ended TDR
  - ❑ Differential Cross-talk(X-talk) between TX-RX, TX-TX and RX-RX pairs
  - ❑ Optimize the layout structure and demonstrate PKG is conformal to SI requirements
- ❑ Extract the S-parameter model for the improved design.



DDR3 memory interface (east side only): 50Ω DQ & 100Ω Differential DQS @ 1.6Gbps

- ❑ Verify DQ* to DQ* in-byte delay mismatch and DQ*byte to its DQS* clock delay mismatch
- ❑ Re-route signals in layout, if necessary, to meet signal delay match requirements
- ❑ Extract and provide S-parameter model of the package design to be later used for transient analysis
- ❑ Compare results from the extracted model with frequency domain package requirements
  - ❑ Differential & SE IL and RL
  - ❑ SE DQ* to DQ* Cross-talk





APTE iMAPS ROMANIA · UPSEE UP-SKILL ENGINEERING EDUCATION · MICROCHIP · NXP

TIEμ 2nd Edition

Technologies of Interconnections in Electronics
Registration

Transilvania University of Brasov

2nd - 5th April 2024

Contest Webpage: https://eecamp.eu/tie-micro/

Registration Form: https://forms.office.com/e/tPBrG2WRx1

Registration Deadline: 12th of March 2025

Before the contest starts you will receive access to the layout design/ simulation tool chosen in the Registration Form!

APTE iMAPS ROMANIA UPSEE UP-SKILL ENGINEERING EDUCATION MICROCHIP NXP