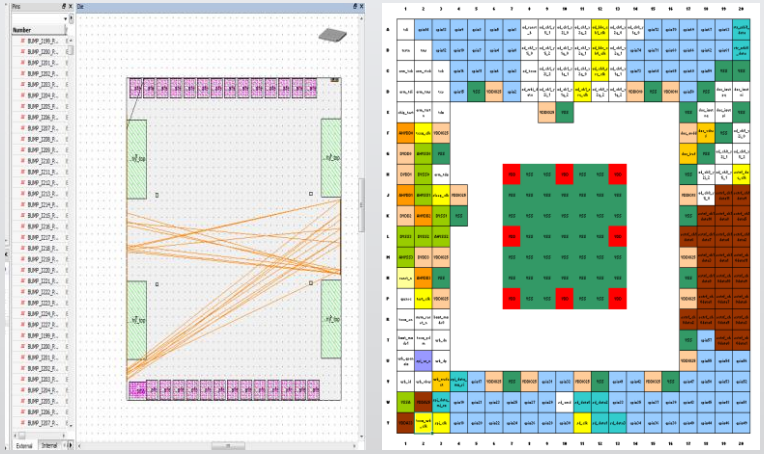
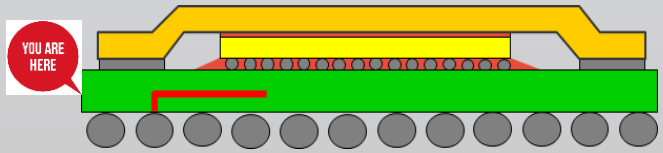
TIE$_\mu$ 2024 – Subject Overview

UNIVERSITATEA LUCIAN BLAGA DIN SIBIU

24th of April 2024





(For illustration purposes, not the actual package)

Context:

- You are a fresh Package Design engineer about to receive their first assignment. Your team is working on an ASIC project for an external customer, and you are tasked with executing and analyzing the package layout

Challenge:

- Your mission is to address both layout and electrical simulation phases of the package design, ensuring that your work meets all the required electrical and manufacturing specifications
- In the layout phase, you will receive a feasibility study that already determined a routing strategy and technology selection, that you will need to refine in order to prepare the design for manufacturing.
- During the simulation phase, you will need to conduct rigorous signal and power integrity simulations, detecting any potential issues that could compromise the package performance.
- Your objective is to finalize the design following the fabrication rules and run relevant electrical checks to validate your layout will meet the required specifications, thereby ensuring the electronic module meets the requirements necessary for flawless functionality.

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TIE$_\mu$ 2024 – Subject Requirements

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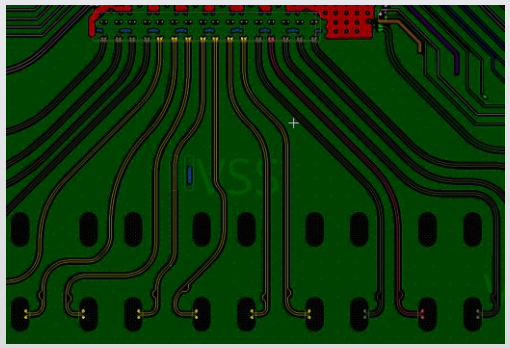

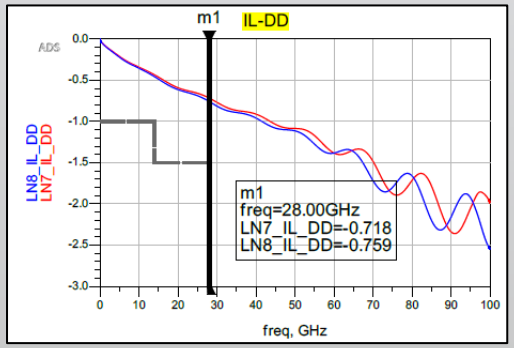

(For illustration purposes, not the actual package)

I. Package Layout:

- Review the initial feasibility routing layout that was provided to you and make sure it corresponds with the latest customer inputs. *This includes checking the pin maps in the initial design are accurate, the impedances used in the initial study are following current specifications*
- Complete the layout while making sure you are using the provided manufacturing rules.
  Use layout guidelines and best practices to get to a fully routed design ready for simulations.

II. Post-Layout Analysis:

- Utilize your layout design (or the checkpoint provided layout) to implement a comprehensive SI and PDN extraction. *Evaluate electrical performance based on the project electrical specifications for each critical interface.*
- Based on the evaluation results, implement layout optimizations and reassess updated electrical performance of your design. *Adjust high speed transitions, critical power paths, return paths if needed.*

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TIE$_\mu$ 2024 – Registration

Contest Webpage: https://eecamp.eu/tie-micro/

Registration Form: https://forms.office.com/e/EjwQErWuPz

Before the contest starts you will receive access to the layout design/ simulation tool chosen in the Registration Form!

Independent of your contest participation, you can always request Student License Access from here:

cadence https://www.cadence.com/en_US/home/company/cadence-academic-network/contact-us.html

Ansys https://www.ansys.com/academic/students/ansys-electronics-desktop-student