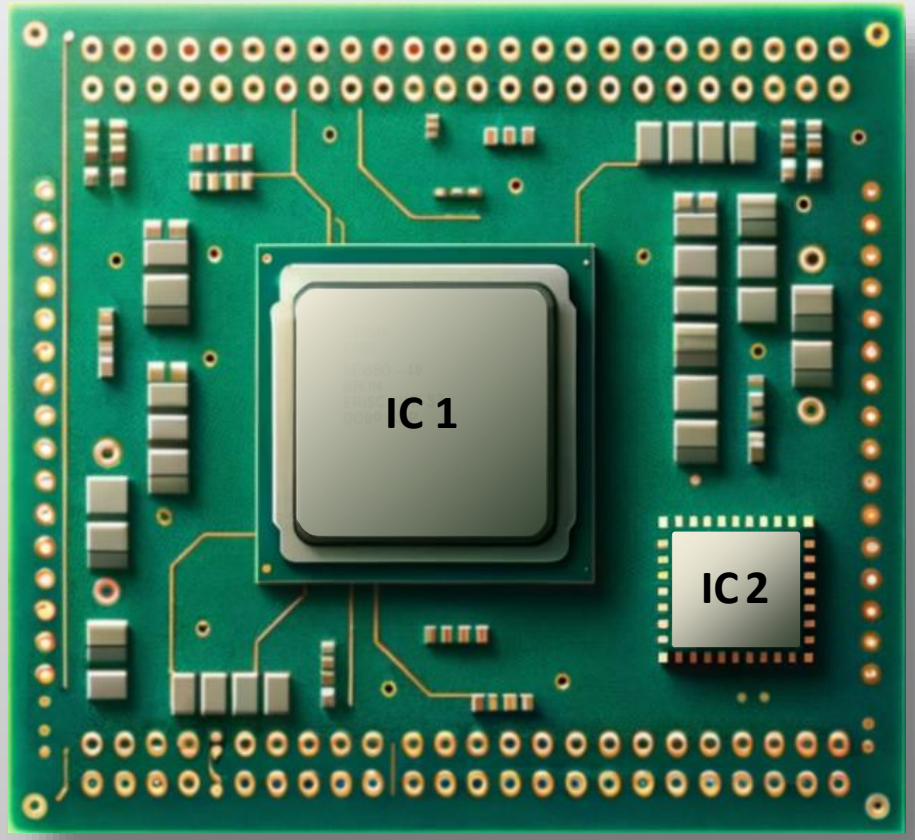
TIE plus 2024 – Subject Overview

UNIVERSITATEA LUCIAN BLAGA DIN SIBIU

24th of April 2024



(For illustration purposes, not the actual PCB)

Context:

- You are a Junior Signal Integrity Engineer part of a team tasked with designing a High-Performance Embedded SoM product destined for compute-intensive edge processing applications.

Challenge:

- Your mission is to address both pre-layout and post-layout phases of the PCB design, ensuring that signal integrity is maintained throughout the module's operation.
- In the pre-layout phase, you must devise a routing strategy that optimizes signal paths and minimizes interference.
- During the post-layout phase, you will need to conduct rigorous signal integrity simulations, detecting any potential issues that could compromise the module's performance.
- Your objective is to detect and correct any design-related issues, thereby ensuring the electronic module meets the requirements necessary for flawless functionality.

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TIE plus 2024 – Subject Requirements

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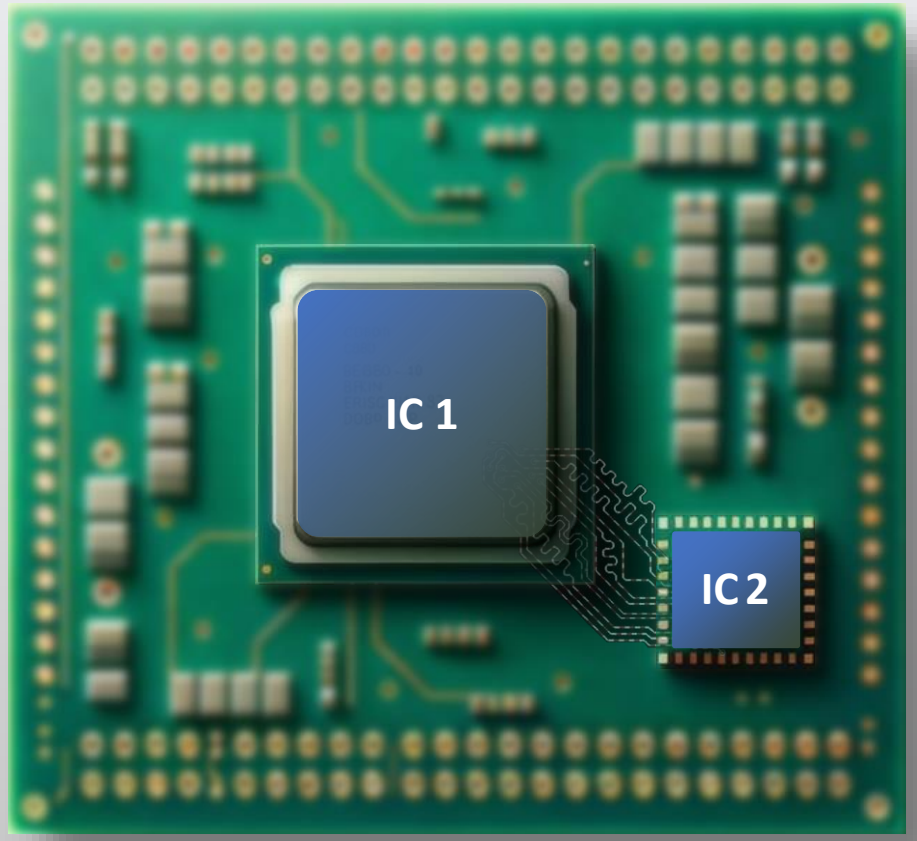

(For illustration purposes, not the actual PCB)

I. Pre-Layout Analysis:

- Based on the provided PCB stack-up, define the routing strategy and layout design directives for a high-speed parallel link interface. *This includes selecting the routing layers, designing via transitions, defining trace width and spacing, and establishing the maximum allowed trace length skew.*
- Model the communication channel and perform all necessary transient simulations to ensure signal quality and interface timing. *Analyze signal reflections, crosstalk levels, and eye diagram at the receiver.*

II. Post-Layout Analysis:

- Utilize the provided PCB layout design to realize a comprehensive transient simulation to validate signal integrity & synchronization. *Evaluate performance based on design targets established during Pre-Layout.*
- Based on the evaluation results, define corrective measures for the layout design if satisfactory design margin is not achieved. *Adjust trace width, spacing, length and/ or via transitions if needed.*

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TIE plus 2024 – Registration

Contest Webpage: https://eecamp.eu/tieplus/

Registration Form: https://forms.office.com/e/J6dEj3hYjt

Simulation Software Student License Access:

SIMULIA CST STUDIO SUITE — https://edu.3ds.com/en/software/cst-studio-suite-learning-edition

Ansys ELETRONICS DESKTOP — https://www.ansys.com/academic/students/ansys-electronics-desktop-student

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