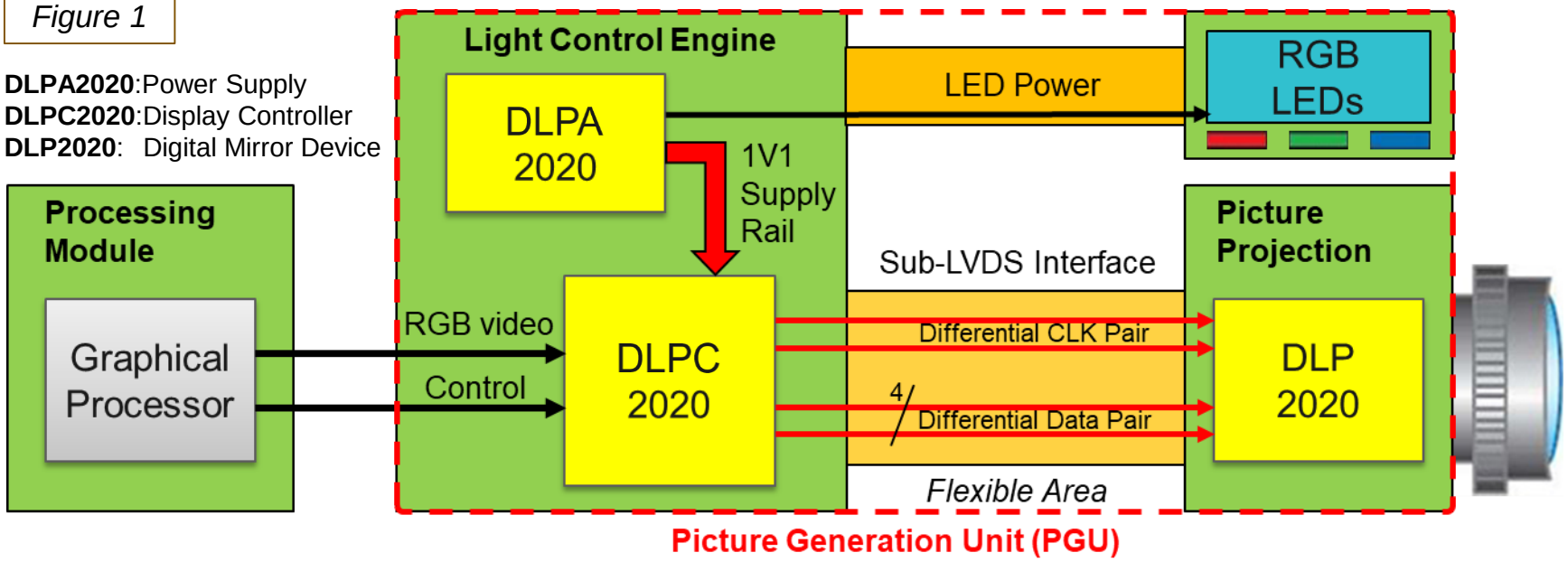
TIEplus 2020 Subject

- The diagram below describes a simplified architecture of an augmented reality headset system divided in 3 functional modules: *Processing Module*, *Light-Control* and *Picture-Projection*.

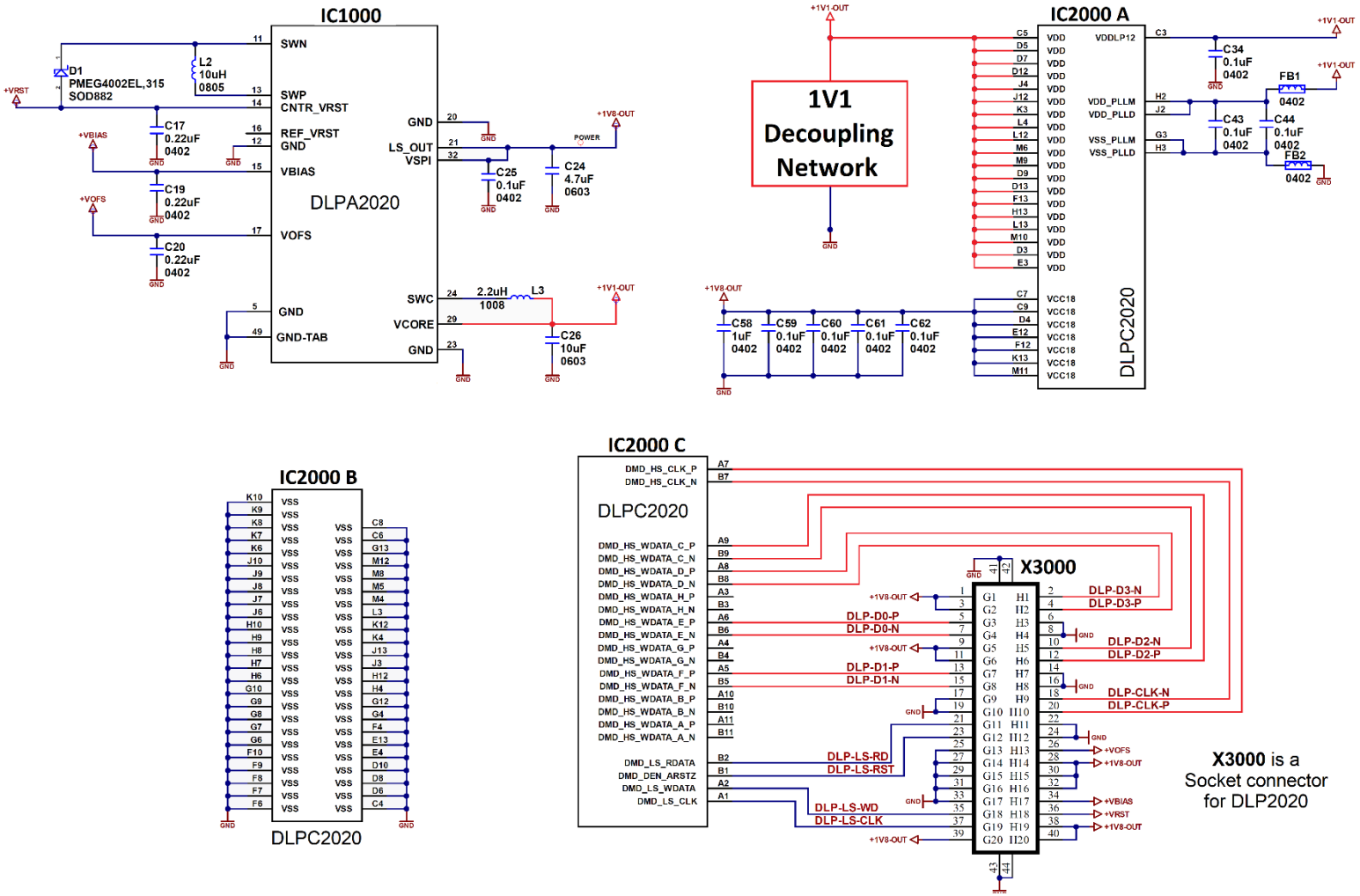
Figure 1

DLPA2020:Power Supply
DLPC2020:Display Controller
DLP2020: Digital Mirror Device



- The challenge is to design the critical electrical connections within the *Light-Control Engine* and *Picture-Projection* modules, which together form the **Picture Generation Unit (PGU)**.
- The entire system will be designed on a single PCB in rigid-flex technology with Polymide based substrate for the flexible areas.

TIEplus 2020 Schematic



TIEplus 2020 Requirements

A) Signal Integrity of the Sub-LVDS video interface

1. Based on the provided PCB stack-up provided in figure 2, define the routing directives and strategy for the Sub-LVDS video interface. This includes selecting the routing layers, trace width and spacing, inter-pair spacing and layer transitions.

2. Define a differential via design pattern to match the differential pair routing impedance.

3. Evaluate intra-pair skew requirements and define length matching restrictions.

4. Route the Sub-LVDS lines and associated reference planes in a CAD environment considering the component placement in figure 3.

5. Evaluate signal quality.

6. Evaluate interface timing.

7. Optimize routing if necessary.

TIEplus 2020 Requirements

B) Power Integrity of the 1V1 Core Supply Rail

1. Analyze the thermal distribution of the **PGU** board based on equivalent thermal network provided in figure 4.

2. Evaluate noise budget and define DC drop and AC design targets.

3. Define power supply rail routing directives.

4. Define capacitor decoupling network based on AC design target.

5. Route the power rails for 1V1 and GND (including capacitor network) in a CAD environment, considering the component placement in figure 3.

6. Evaluate PDN performance (post-layout) using appropriate simulations in both DC and AC domains. Optimize layout to meet design targets.

* Consider the thermal distribution impact on PCB and component performance for the power integrity analysis.

*Use capacitor models from Murata MLCC lineup (www.murata.com)
*Only capacitors with 0402, 0603 and 0805 case type must be used for decoupling

TIEplus 2020
Modeling Information

Model	File	Notes
DLPA2020 VRM Model	-	VRM model provided in slide 6
DLPC2020 IBIS	DLPC2020.ibs	
DLP2020 IBIS	DLP2020.ibs	IBIS model does not contain internal differential termination resistor
DLPA2020 Datasheet	DLPA2020.pdf	
DLPC2020 Datasheet	DLPC2020.pdf	
DLP2020 Datasheet	DLP2020.pdf	
PCB Stack-up	-	Stack-up provided in slide 7
X3000 socket Datasheet & Simulation model	AXT540124.pdf	
	AXT540124.s40p	Model pinout provided in slide 10

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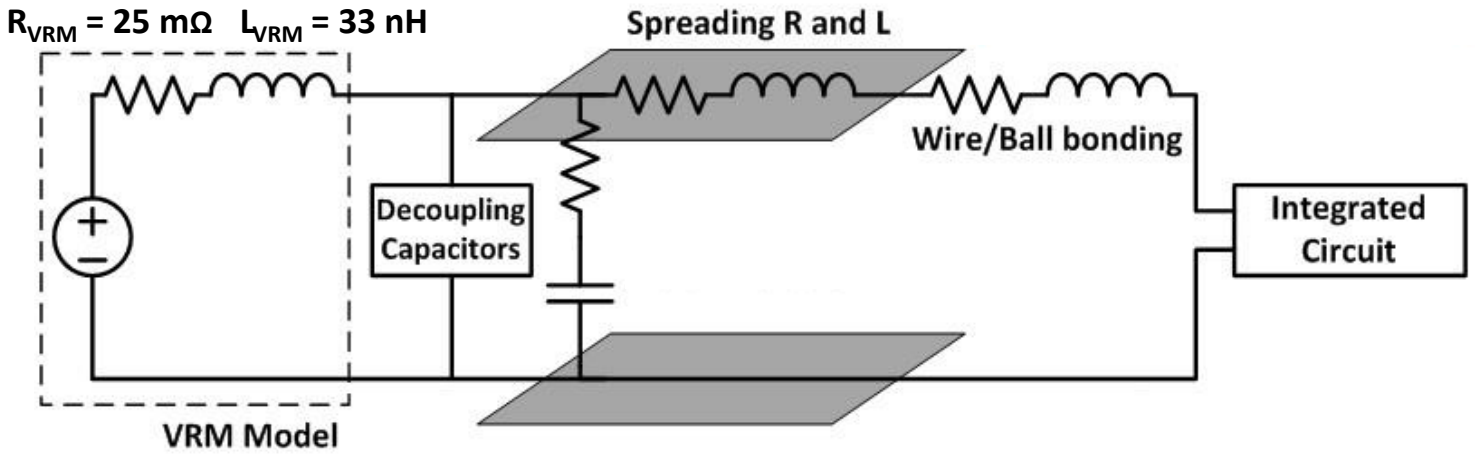
DLPA2020 – VRM Modeling

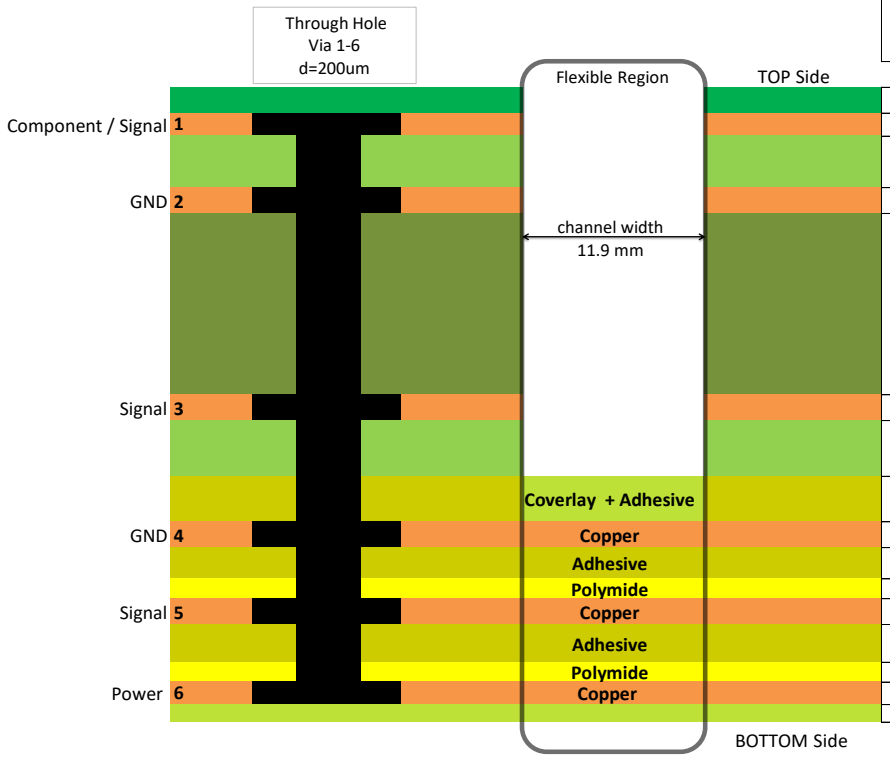
- **Output Voltage: 1.1 [V]** (net +***1V1-OUT***)
- **Output Switching Ripple: 10 [mVpp]**
- **DC output voltage accuracy: ±1.5%**
- **Power Dissipation: 1.6W**

VRM Modeling:



TIEplus 2020
PCB Stack-up

Figure 2



		Nominal Thickness [um]	Final Thickness (after pressing)	Type	Dk 1MHz	Dk 1GHz	Dk 10GHz	Df 1MHz	Df 1GHz	Df 10GHz
		20	20	Solder Mask		3.8				
Component / Signal	1	43	43	18um copper + plating						
		114	114	2116 type Prepreg		4.25	4.13		0.0156	0.0186
GND	2	18	18	18um base copper						
		914	914	36 mil FR4 CORE		4.47	4.34		0.0147	0.0175
Signal	3	18	18	18um base copper						
		114	105	2116 type Prepreg		4.25	4.13		0.0156	0.0186
		75	75	Polyimide Adhesive prepreg (no flow)	3.2		3.2	0.0015		0.0015
GND	4	18	18	18um base copper						
		50	50	Polyimide Adhesive	3.2		3.2	0.0015		0.0015
		25	25	Polymide Laminate	3.4		3.2	0.002		0.003
Signal	5	18	18	18um base copper						
		75	66	Polyimide Adhesive	3.2		3.2	0.0015		0.0015
		25	25	Polymide Laminate	3.4		3.2	0.002		0.003
Power	6	43	43	18um base copper + plating						
		25	25	Coverlay	3.2		3.2	0.0015		0.0015
		1595	**1577**							

TIEplus 2020 CAD Drawing

Notes:

- Only the following components are mandatory for layout design: IC1000, IC2000, X3000(socket)
- Placement for IC1000 and IC2000 is fixed based on fig. 3
- 1V1 routing only allowed on outer layers
- All dimension in millimeters

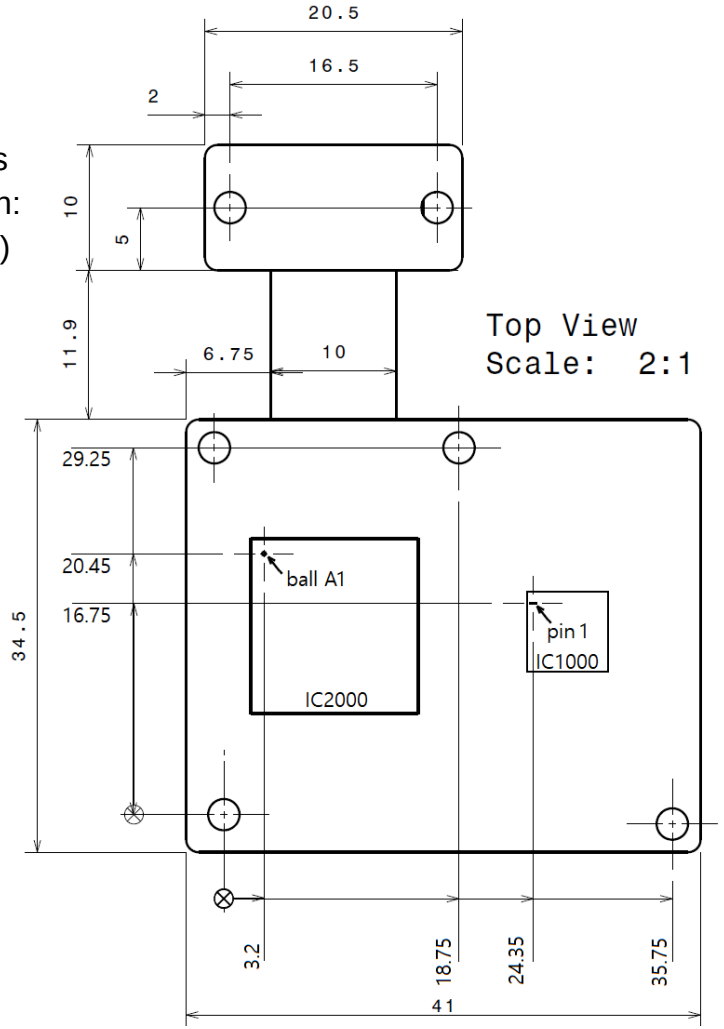
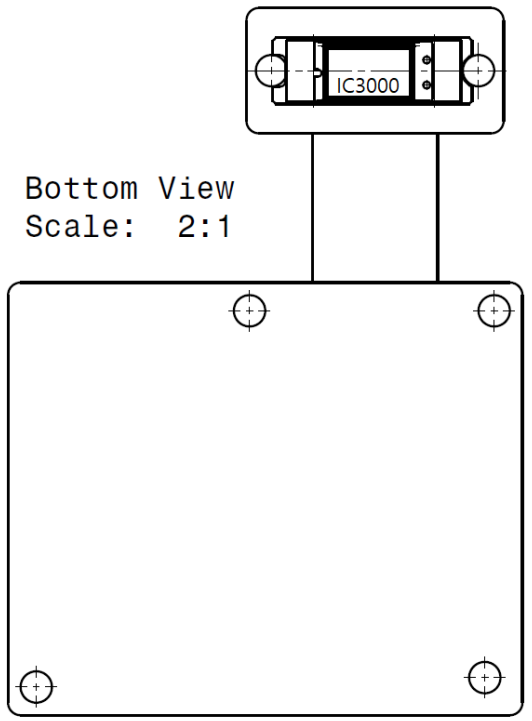


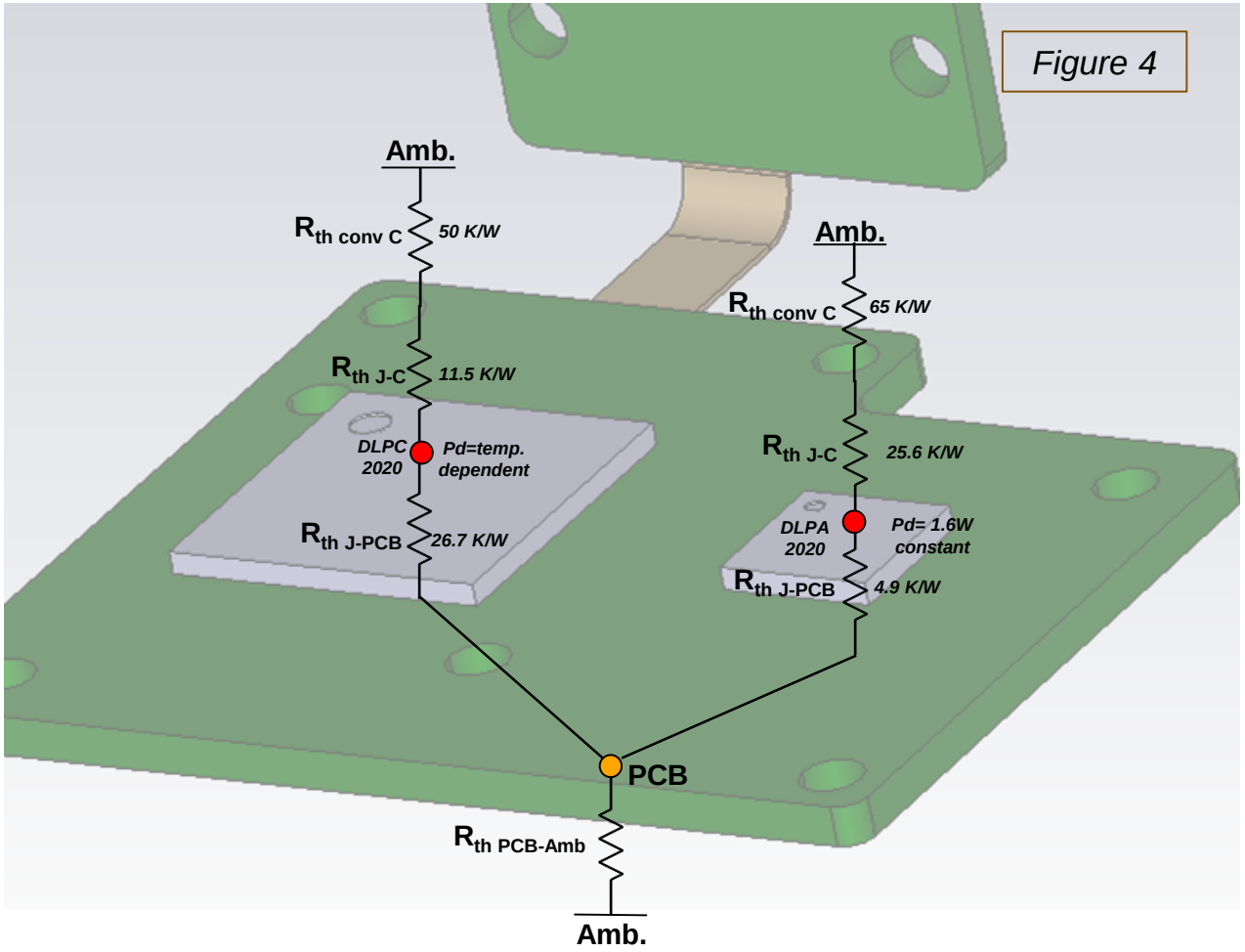
Figure 3



TIEplus 2020 Thermal Network

Notes on thermal modeling:

- DLPC2020 power dissipation must be calculated based on datasheet values considering power supply inputs; the value has a strong dependence on the junction temp)
- DLPA2020 power dissipation is fixed at 1.6W
- For modeling simplification, the PCB temperature can be considered uniform.
- Maximum ambient temperature: 55^{o}C



TIEplus 2020
X3000 Touchstone model pinout