TIEplus 2019 Subject

TIEplus
Signal & Power Integrity
Simulation Challenge

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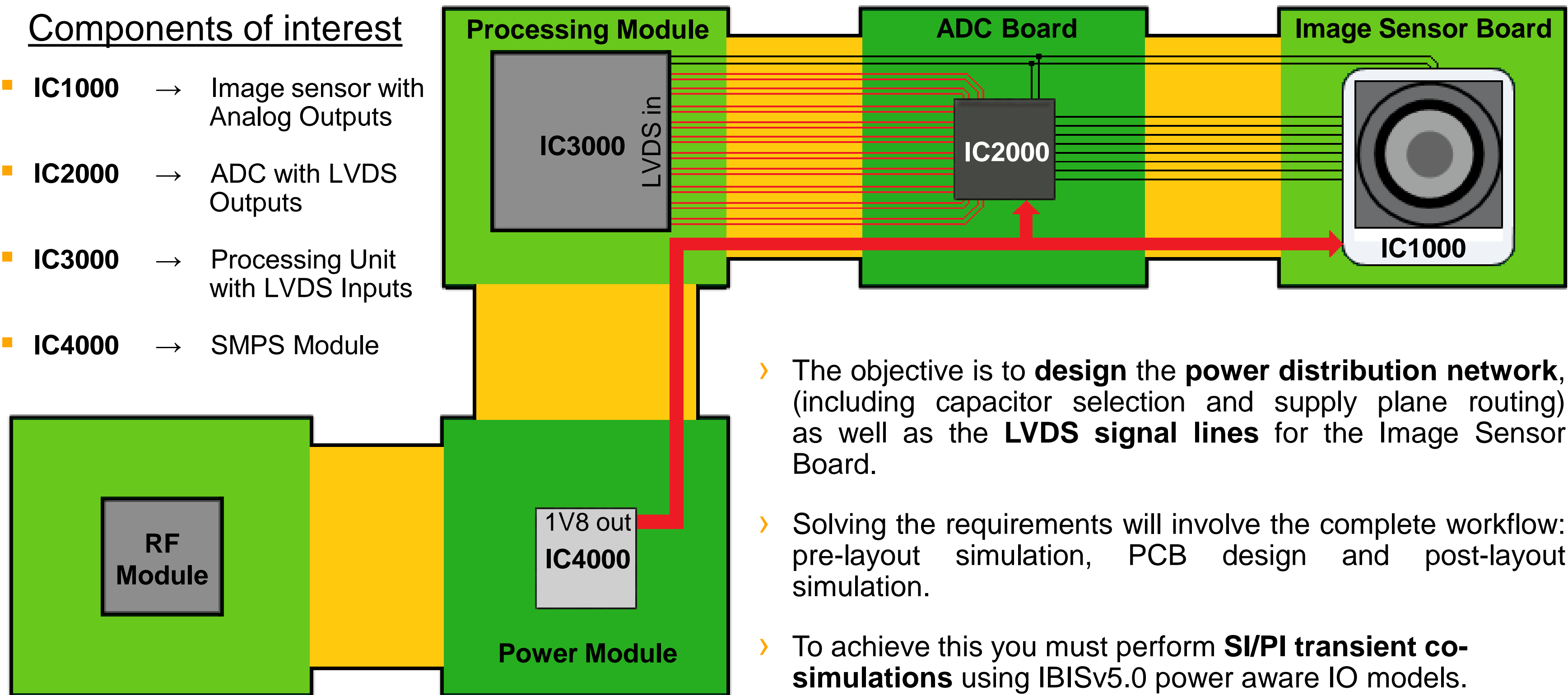
Block Diagram

TIEplus
Signal & Power Integrity Simulation Challenge

› The diagram below describes a simplified architecture of a space cube satellite PCB which is divided in 5 functional modules: RF, Power, Processing, ADC and Image Sensor.



Components of interest

- **IC1000** → Image sensor with Analog Outputs
- **IC2000** → ADC with LVDS Outputs
- **IC3000** → Processing Unit with LVDS Inputs
- **IC4000** → SMPS Module

› The objective is to **design** the **power distribution network**, (including capacitor selection and supply plane routing) as well as the **LVDS signal lines** for the Image Sensor Board.

› Solving the requirements will involve the complete workflow: pre-layout simulation, PCB design and post-layout simulation.

› To achieve this you must perform **SI/PI transient co-simulations** using IBISv5.0 power aware IO models.

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Schematic

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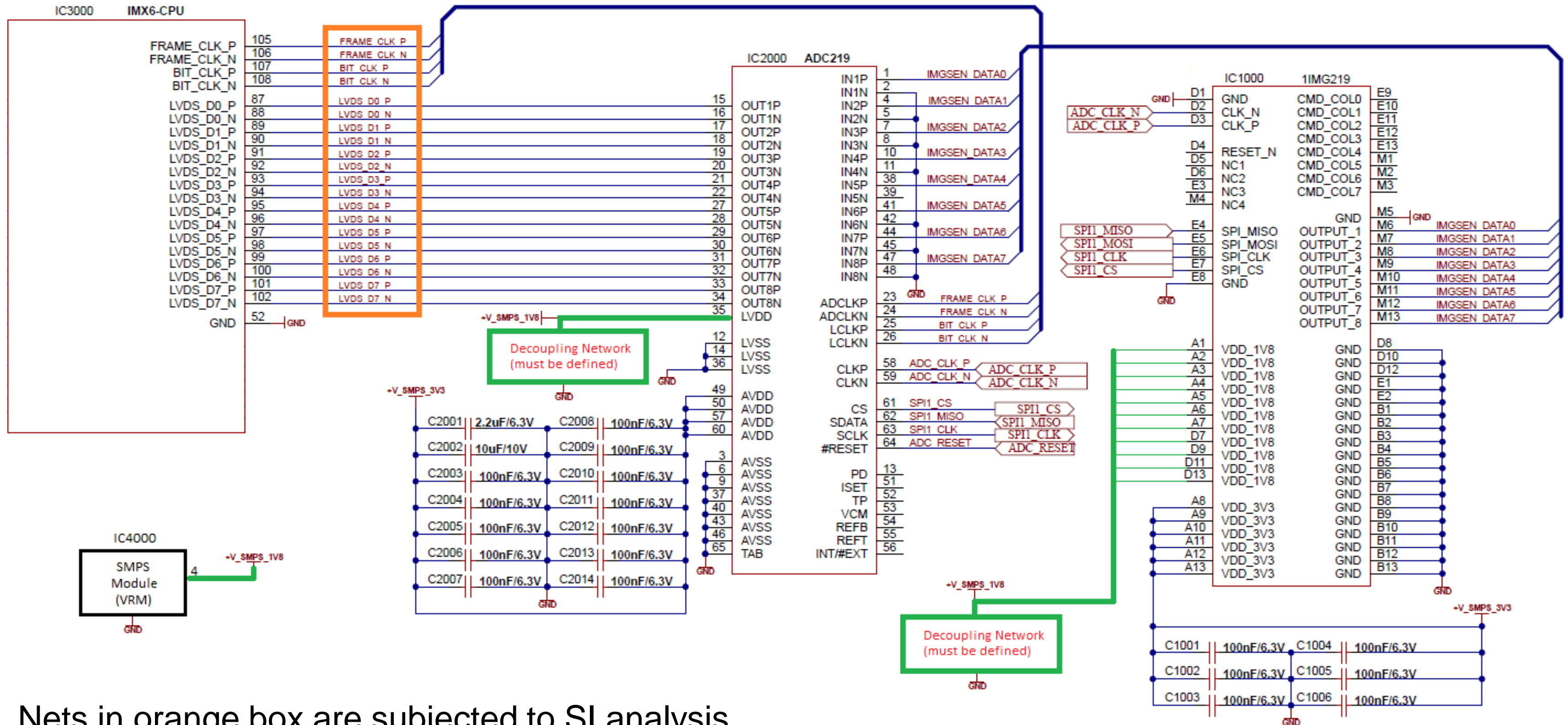

- Nets in orange box are subjected to SI analysis
- Green boxes represent the capacitor decoupling networks that result form the PI design

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Stack-up

TOP Side

Layer	Stack-up	Flex Area Thickness [um]	Rigid Area Thickness [um]	Type	Dk
			20	solder mask	4.2
Signal 1			43	18 copper + 25 plating	
			173	1 x 7628 prepreg	4
GND / Signal 2			43	18 copper + 25 plating	
	Flexible part		300	3 x 2116 prepreg or 2 x 1506 prepreg	4
	Coverlay + Adhesive	50	50	Coverlay	3.5
GND 3	Copper	18	18	18 copper	
	Polymide	75	75	polymide core	3.5
Signal 4	Copper	18	18	18 copper	
	PI Coverlay	50	50	Coverlay	3.5
	Acrylic Adhesive	40	40	Adhesive	
	PI Coverlay	50	50	Coverlay	
GND 5	Copper	18	18	18 copper	
	Polymide	75	75	polymide core	3.5
Power / Signal 6	Copper	18	18	18 copper	
	Coverlay + Adhesive	50	50	Coverlay	3.5
	~ d [mm]		300	3 x 2116 prepreg or 2 x 1506 prepreg	4
GND 7			43	18 copper + 25 plating	
			173	1 x 7628 prepreg	4
Signal 8			43	18 copper + 25 plating	
			20	solder mask	4.2
		462	**1620**		

BOTTOM Side

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PCB Outline

RIGID AREA C — IC3000
RIGID AREA D — IC2000
RIGID AREA E — IC1000
RIGID AREA A
RIGID AREA B — IC4000

60.00mm, 53.00mm, 9.00mm, 3.50mm

- Component placement:
  - Place all components centered inside the corresponding rigid area
  - Define footprint orientation for best routing
- Detailed view of dimensions available in PCB_outline.pdf
- PCB outline in DXF format: PCB_OUTLINE_DXF.dxf

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Modeling data

Model	File	Description
IC1000 on-die capacitance	ic1000_on-die_cap.sp	Image sensor internal decoupling capacitance
IC2000 ibis model	ic2000.ibs	ADC power aware IBIS model for LVDS output buffer
IC2000 on-die capacitance	ic2000_on-die_cap.sp	ADC internal decoupling capacitance
IC3000 ibis model	ic3000.ibs	Processing module IBIS model for LVDS input buffer
IC3000 package model	Ic3000_pkg.s40p	Processing module PCB parasitics for LVDS lines
IC4000 VRM model	VRM_model.sp	Power supply model

Capacitor models can be downloaded from Murata website (GCM series):

- https://ds.murata.co.jp/simsurfing/mlcc.html?lcid=en-us OR
- https://psearch.en.murata.com/capacitor/result/smd/?pid=GCM&pid_method=begin&cat=lineup&status=development

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Requirements

- Design the LVDS channel IC2000->IC3000 to meet signal integrity requirements
  - Define controlled impedance routing guidelines
  - Define length matching requirements
  - Evaluate termination scheme
- Design the power delivery network for 1V8 power rail in order to meet specifications of supply voltage IC1000 and IC2000
  - Evaluate power rail IR Drop and define power plane routing guidelines
  - Define worst-case noise budget at IC power pins (in dynamic current conditions)
  - Define decoupling capacitor network considering the simultaneous switching of all IC2000 LVDS outputs
  - Route the power delivery network (including capacitors) according to findings
- Based on previous findings route the LVDS interface and the power delivery network (including capacitors) for the 1V8 power rail
- Perform post-layout transient SI-PI co-simulation to validate design and optimize if required

*** Pre-layout SI-PI transient co-simulation is required in order to accurately evaluate power supply noise and impact on LVDS signal parameters**