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General circuit description

The multi-board system overview presented in figure 1 is given, describing an high resolution image acquisition system for quality compliance testing. Figure 2 presents the PCB board connectivity and signal flow.

System description:

- Board 1
  - represents the image source device containing the image source driver IC100 (IBIS model: Spartan6.ibs); the high speed interface consists out of 13 (1*CLK + 12*Data) differential pairs following RSDS specifications (Reduced Swing Differential Signaling)
  - the RSDS signals exit Board1 PCB trough connector B1.X100 and are propagated by a flexible ribbon cable to Board 2
  - the Board1 PCB interconnect model is provided as touchstone file
- Board 2
  - represents the an intermediate connectivity board that is used to connect and organize the RSDS lines to match Board 3 requirements
  - this PCB is under development and requires pre-layout routing directives that will result from the signal integrity analysis
  - the PCB stack-up is provided
- Board 3
  - represents a ML605 development board containing a Virtex6 FPGA
  - the receiver for the RSDS signals of interest and is represented by U1, a Virtex6 FPGA (IBIS Model: Virtex6.ibs)
  - PCB CAD data in ODB++ format and stack-up information are provided

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System Overview

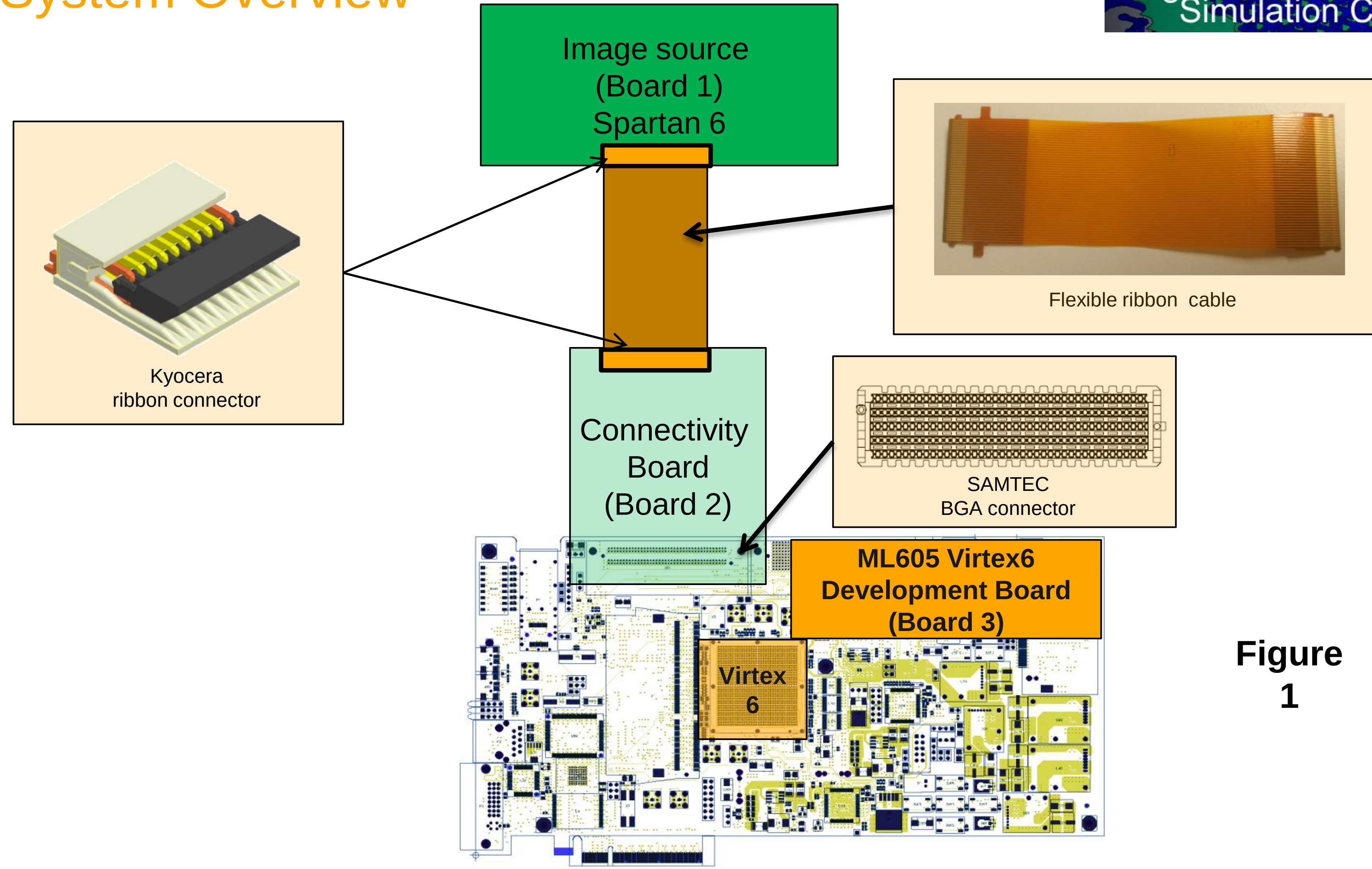

Figure 1

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Multi-board system diagram. Signal flow diagram.

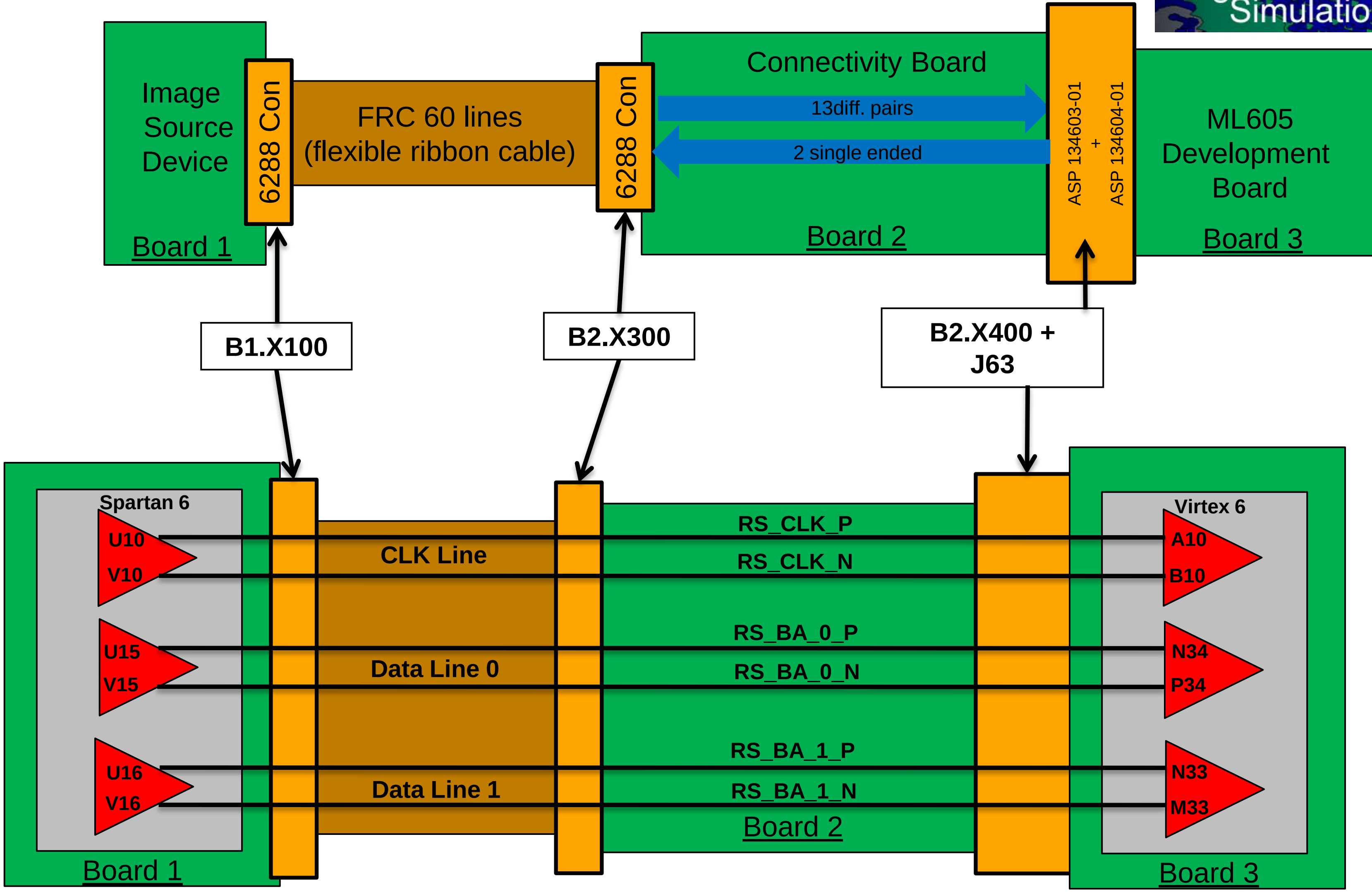

Figure 2

Signals of interest for the simulation

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Requirements

Based on the previous system description it is required to analyze signal integrity aspects for the signals RS_CLK_P, RS_CLK_N, RS_BA_P_0, RS_BA_N_0 , RS_BA_P_1, RS_BA_N_0 based on the signal flow diagram from figure 2.

Requirements

A) Define the routing directives for Board 2 PCB specifying: routing layers, routing topology options (microstrip/stripline), differential and common-mode impedance, inter-pair spacing (spacing between the traces of the same pair), trace width.

B) Evaluate the need of series resistors placement on Board 2 for signal integrity improvements (e.g. reflections, crosstalk) .

C) Evaluate VIA propagation delays on Board 2 and establish if there is a need for inter-pair and pair-to-pair VIA number matching.

D) Evaluate pair-to-pair far-end crosstalk at system level. Define a Vp-p crosstalk vs. pair-to-pair spacing chart. Define the minimum acceptable pair-to-pair spacing for Board 2 based on the obtained data.

E) Evaluate the following signal parameters at receiver end (Virtex6 input pins): rise\fall slew rate SE, overshoot & undershoot values SE, high\low time differential.

F) Evaluate the following timing parameters at receiver end (Virtex6 input pins): setup time to CLK (differential); hold time to CLK (differential)

* All simulation data must be provided for MIN (slow), TYP(typical), MAX(fast) IBIS model PVT IBIS corners (assume the logical worst case for the target analysis)

Simulation conditions:

CLK frequency: 125MHz, duty cycle: 50%
Single Data Rate transfer (positive edge)
Unit Interval =1 *CLK period = 8ns

Receiver signal requirements:

Data-to-CLK max. pair-to-pair skew = +/- 50 ps
Max. inter-pair skew = +/- 10 ps
Max. differential signal crosstalk =10 mVpp
High Input Voltage = +100mV
Low Input Voltage = -100mV